ABSTRACT OF THE DISCLOSURE

A pattern generator includes an address generator, an address topology generator, and a data topology generator. The address generator is adapted to provide a first address having a plurality of address bits. The address topology generator includes a first plurality of programmable logic gates. Each programmable logic gate of the first plurality is coupled to receive at least a subset of the plurality of address bits. The first plurality of programmable logic gates generate a second address having a plurality of modified address bits. The data topology generator is adapted to receive at least a subset of the plurality of modified address bits and generate write data based on the subset of modified address bits. A method for generating a pattern includes generating a first address having a plurality of address bits. A second address having a plurality of modified address bits is generated. The second address is a programmable combination of subsets of the address bits. Write data is generated based on a subset of the modified address bits.